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U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

DOCKET #: 4925-131PUS

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

				U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
				09/889522

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/00116	11 January 2000	22 January 1999

TITLE OF INVENTION

An ATM Inband Protocol

APPLICANT(S) FOR DO/EO/US

Hubertus STORCK

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371
3. [x] This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [x] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [x] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [x] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [x] has been transmitted by the International Bureau.
   c. [] is not required, as the application was filed in the United States Receiving Office (RO/US)
6. [] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [x] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [x] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [] have been transmitted by the International Bureau.
   c. [] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [] have not been made and will not be made.
8. [] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). **Unexecuted**
10. [] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. Below concern other document(s) or information included:

11. [x] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [x] A **FIRST** preliminary amendment.
    [] A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. [] A substitute specification.
15. [] A change of power of attorney and/or address letter.
16. [x] Other items or information *(specify)*: PCT Publication Sheet, Int'l Preliminary Examination Report, Written Opinion, Reply to Written Opinion, Int'l Search Report, PCT Request, Notice Informing the Applicant of the Communication of the International Application to the Designated Offices, Communication Requesting Change of Address of the Applicant

U.S. APPLICATION NO (If known, see 37 CFR 1.5) 09/889522	INTERNATIONAL APPLICATION NO PCT/EP00/00116	ATTORNEY'S DOCKET NUMBER 4925-131PUS

17.[x]The following fees are submitted:		
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO ..... **$860.00** International preliminary examination fee paid to USPTO (37 CFR 1.482)..... **$690.00** No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))..... **$710.00** Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ..... **$1000.00** International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$**	860
Surcharge of **$130.00** for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	**$**	

Claims	Number Filed	Number Extra	Rate		
Total Claims	51 - 20 =	31	x **$18.00**	**$**	558
Independent Claims	6 - 3 =	3	x **$80.00**	$	240
Multiple dependent claim(s) (if applicable)			+ **$270.00**	**$**	
TOTAL OF ABOVE CALCULATIONS =				**$**	1658
Reduction of ½ for filing by small entity, if applicable.				**$**	
SUBTOTAL =				**$**	1658
Processing fee of **$130.00** for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				**$**	
TOTAL NATIONAL FEE =				**$**	1658
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by the appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				**$**	
TOTAL FEES ENCLOSED					$1658
Amount to be refunded:					**$**
charged:					**$**

a. [x] One check in the amount of $ 1658 to cover the above fee is enclosed.
b. [] Please charge my Deposit Account No. 03-2412 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. [x] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 03-2412. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO.
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09/889522

By Express Mail #EL895344028US
Attorney Docket # 4925-131PUS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re National Phase PCT Application of
Hubertus STORCK et al.
Int'l PCT Appln. No.: PCT/EP00/00116
Int'l Filing Date: 11 January 2000
For: An ATM Inband Protocol

Check box if applicable:
☐ DUPLICATE

GENERAL AUTHORIZATION FOR PAYMENT OF FEES AND PETITIONS FOR EXTENSIONS OF TIME
Submit an original and a duplicate for fee processing

Assistant Commissioner for Patents
BOX PCT
Washington, DC 20231

Sir:

The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 03-2412

[X] Any filing fees required under 37 CFR §1.16.
[X] Any patent application processing fees under 37 CFR §1.17 not otherwise paid by check.
[X] The issue fee set in 37 CFR 1.18 at 3 months from mailing of the Notice of Allowance, pursuant to 37 CFR 1.311 (b) provided the fee has not already been paid by check.
[X] Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,
COHEN, PONTANI, LIEBERMAN & PAVANE

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Dated: July 17, 2001

By Express Mail # EL895344028US · July 17, 2001

Attorney Docket # 4925-131PUS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re National Phase PCT Application of
Hubertus STORCK et al.
International Appln. No.: PCT/EP00/00116
International Filing Date: 11 January 2000
For: An ATM Inband Protocol

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231
BOX PCT

S I R:

Prior to examination of the above-identified application please amend the application as follows:

IN THE CLAIMS:

Amend claims 3-6, 8, 9, 11-13, 16, 17, 21, 26, 30, and 34-36 to read as follows:

3. (Amended) A process according to claim 1, characterised in that the devices (4) are ATM interface units of the physical layer by means of which a data path interface (7) provides access for the ATM layer to a physical transmission medium.

4. (Amended) A process according to claim 1, characterised in that addressing of ATM cells to the control unit (5) by the management unit (1) takes place via a VPI/VCI address associated with the control unit (5), or if the management unit (1) communicates directly with the control unit (5), via an UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

5. (Amended) A process according to claim 1, characterised in that addressing of ATM cells to the management unit (1) by the control unit (5) takes place via a VPI/VCI address associated with the management unit (1), or if the management unit (1) communicates directly with the control unit (5), via a UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

6. (Amended) A process according to claim 1, characterised in that transmission of the ATM cells is based on the request-response protocol.

8. (Amended) A process according to claim 1, characterised in that prior to any forwarding of ATM cells destined for the management unit (1), the control unit (5) forms a checksum, and prior to any forwarding of ATM cells destined for a control unit (5), the management unit (1) forms a checksum, across at least part of the payload of the ATM cell and integrates this sum into the ATM cell to be transmitted.

9. (Amended) A process according to claim 1, characterised in that prior to carrying out any instructions, the control unit (5) checks a checksum transmitted with the ATM cell received, and carries out the instructions only if no transmission error is detected; otherwise it discards the ATM cell and is ready to receive new ATM cells.

11. (Amended) A process according to claim 8, characterised in that

- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum, the management unit (1) sends the same ATM cell again, identifying it as a repetition cell;
- when receiving a repetition cell, the control unit (5) checks whether or not, following the first ATM cell, a response ATM cell was transmitted to the management unit (1); and
- if no, processes the instructions contained in the cell; or
- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

12. (Amended) A process according to claim 1, characterised in that for each ATM cell to be composed, the control unit (5) maps the current interrupt state of the connected devices (4) into interrupt bits provided for this purpose in the payload of the ATM cell.

13. (Amended) A process according to claim 1, characterised in that the control unit (5) autonomously and regularly reads in data from devices (4) connected to it and transmits such data, integrated into ATM cells, to the management unit (1).

16. (Amended) A control unit (5) according to claim 14, characterised in that the data path interface (7) corresponds to the data path interface specified in Appendix 2 of Utopia Level 2.

17. (Amended) A control unit (5) according to claim 14, characterised in that it is suitable for composing the register data read from the registers of the devices (4) to become ATM cells, address it to a management unit (1) by means of the VPI/VCI address of the management unit (1), or address it using a UTOPIA address reserved for inband communication, and forward it to the data path interface (7).

21. (Amended) A management system according to claim 19, characterised in that the devices (4) comprising registers are ATM interface units of the physical layer by way of which the ATM layer of the ATM network has access to at least one transmission medium.

26. (Amended) An ATM cell according to claim 23, characterised in that a "big endian order" is used.

30. (Amended) A method according to claim 27, characterised in that a "big endian order" is used for the ATM cell.

34. (Amended) Management unit according to claim 31, characterized in that the means are suited for using a "big endian order".

35. (Amended) The use of an ATM cell according to claim 23 for configuring ATM interface units (4) of the physical layer.

36. (Amended) The use of an ATM cell according to claim 23 for the reading out of data available in the ATM interface units (4) of the physical layer.

Add the following new claims:

37. (New) A process according to claim 2, characterised in that the devices (4) are ATM interface units of the physical layer by means of which a data path interface (7) provides access for the ATM layer to a physical transmission medium.

38. (New) A process according to claim 2, characterised in that addressing of ATM cells to the control unit (5) by the management unit (1) takes place via a VPI/VCI address associated with the control unit (5), or if the management unit (1) communicates directly with

the control unit (5), via an UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

39. (New) A process according to claim 2, characterised in that addressing of ATM cells to the management unit (1) by the control unit (5) takes place via a VPI/VCI address associated with the management unit (1), or if the management unit (1) communicates directly with the control unit (5), via a UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

40. (New) A process according to claim 2, characterised in that transmission of the ATM cells is based on the request-response protocol.

41. (New) A process according to claim 40, characterised in that the management unit (1) does not send any further ATM cells to a control unit (5) as long as it has not received a correct response to the preceding ATM cell from said control unit (5), or as long as a time limit has not been exceeded.

42. (New) A process according to claim 2, characterised in that prior to any forwarding of ATM cells destined for the management unit (1), the control unit (5) forms a checksum, and prior to any forwarding of ATM cells destined for a control unit (5), the

management unit (1) forms a checksum, across at least part of the payload of the ATM cell and integrates this sum into the ATM cell to be transmitted.

43. (New) A process according to claim 2, characterised in that prior to carrying out any instructions, the control unit (5) checks a checksum transmitted with the ATM cell received, and carries out the instructions only if no transmission error is detected; otherwise it discards the ATM cell and is ready to receive new ATM cells.

44. (New) A process according to claim 43, characterised in that after each processing of the instructions of an ATM cell, the control unit (5) places at least part of the updated content of the cell to be transmitted to a management unit into an intermediate memory.

45. (New) A process according to of claim 42, characterised in that

- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum, the management unit (1) sends the same ATM cell again, identifying it as a repetition cell;
- when receiving a repetition cell, the control unit (5) checks whether or not, following the first ATM cell, a response ATM cell was transmitted to the management unit (1); and
- if no, processes the instructions contained in the cell; or

- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

46. (New) A process according to claims 9, characterised in that

- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum, the management unit (1) sends the same ATM cell again, identifying it as a repetition cell;
- when receiving a repetition cell, the control unit (5) checks whether or not, following the first ATM cell, a response ATM cell was transmitted to the management unit (1); and
- if no, processes the instructions contained in the cell; or
- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

47. (New) A process according to claim 43, characterised in that

- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum, the management unit (1) sends the same ATM cell again, identifying it as a repetition cell;
- when receiving a repetition cell, the control unit (5) checks whether or not, following

the first ATM cell, a response ATM cell was transmitted to the management unit (1); and

- if no, processes the instructions contained in the cell; or
- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

48. (New) A process according to claim 2, characterised in that for each ATM cell to be composed, the control unit (5) maps the current interrupt state of the connected devices (4) into interrupt bits provided for this purpose in the payload of the ATM cell.

49. (New) A process according to claim 2, characterised in that the control unit (5) autonomously and regularly reads in data from devices (4) connected to it and transmits such data, integrated into ATM cells, to the management unit (1).

50. (New) A control unit (5) according to claim 15, characterised in that the data path interface (7) corresponds to the data path interface specified in Appendix 2 of Utopia Level 2.

51. (New) A management system according to claim 20, characterised in that the devices (4) comprising registers are ATM interface units of the physical layer by way of which the ATM layer of the ATM network has access to at least one transmission medium.

REMARKS

This preliminary amendment is presented to place the application in proper form for examination and to eliminate multiple dependency from the present claims. No new matter has been added. Early examination and favorable consideration of the above-identified application is earnestly solicited.

Attached hereto is a mark-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Any additional fees or charges required at this time in connection with the application may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,
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17 July 2001

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 4, 5, 6, 7 and 8 have been amended as follows:

3. (Amended) A process according to claim 1 [or 2], characterised in that the devices (4) are ATM interface units of the physical layer by means of which a data path interface (7)[, in particular UTOPIA,] provides access for the ATM layer to a physical transmission medium.

4. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that addressing of ATM cells to the control unit (5) by the management unit (1) takes place via a VPI/VCI address associated with the control unit (5), or if the management unit (1) communicates directly with the control unit (5), via an UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

5. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that addressing of ATM cells to the management unit (1) by the control unit (5) takes place via a VPI/VCI address associated with the management unit (1), or if the management unit (1) communicates directly with the control unit (5), via a UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

6. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that transmission of the ATM cells is based on the request-response protocol.

8. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that prior to any forwarding of ATM cells destined for the management unit (1), the control unit (5) forms a checksum, and prior to any forwarding of ATM cells destined for a control unit (5), the management unit (1) forms a checksum, across at least part of the payload of the ATM cell[, in particular a CRC-1O sum,] and integrates this sum into the ATM cell to be transmitted.

9. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that prior to carrying out any instructions, the control unit (5) checks a checksum transmitted with the ATM cell received, and carries out the instructions only if no transmission error is detected; otherwise it discards the ATM cell and is ready to receive new ATM cells.

11. (Amended) A process according to [one of claims 8 - 10] claim 8, characterised in that

- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum, the management unit (1) sends the same ATM cell again,

identifying it as a repetition cell;

- when receiving a repetition cell, the control unit (5) checks whether or not, following the first ATM cell, a response ATM cell was transmitted to the management unit (1); and
- if no, processes the instructions contained in the cell; or
- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

12. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that for each ATM cell to be composed, the control unit (5) maps the current interrupt state of the connected devices (4) into interrupt bits provided for this purpose in the payload of the ATM cell.

13. (Amended) A process according to [one of the preceding claims] claim 1, characterised in that the control unit (5) autonomously and regularly reads in data from devices (4) connected to it and transmits such data, integrated into ATM cells, to the management unit (1).

16. (Amended) A control unit (5) according to claim 14 [or 15], characterised in that the data path interface (7) corresponds to the data path interface specified in Appendix 2 of Utopia Level 2.

17. (Amended) A control unit (5) according to [one of] claim 14 [- 16], characterised in that it is suitable for composing the register data read from the registers of the devices (4) to become ATM cells, address it to a management unit (1) by means of the VPI/VCI address of the management unit (1), or address it using a UTOPIA address reserved for inband communication, and forward it to the data path interface (7).

21. (Amended) A management system according to claim 19 [or 20], characterised in that the devices (4) comprising registers are ATM interface units of the physical layer[, in particular PHYs], by way of which the ATM layer of the ATM network has access to at least one transmission medium.

26. (Amended) An ATM cell according to [one of claims] claim 23 [- 25], characterised in that a "big endian order" is used.

30. (Amended) A method according to [claims] claim 27 [- 29], characterised in that a "big endian order" is used for the ATM cell.

34. (Amended) Management unit according to [one of claims] claim 31 [- 33], characterized in that the means are suited for using a "big endian order".

35. (Amended) The use of an ATM cell according to [one of claims] claim 23 [-34] for configuring ATM interface units (4) of the physical layer.

36. (Amended) The use of an ATM cell according to [one of claims] claim 23 [-34] for the reading out of data[,] available in the ATM interface units (4) of the physical layer[, in particular register values].

SC/wy 981040WO

A process for configuring or monitoring devices comprising registers as well as a control unit and an ATM cell

The invention relates to a process for configuring or reading-out data from devices comprising registers. The invention also relates to a control unit and its integration into a management system for an ATM network for configuring and/or monitoring such devices, as well as an ATM cell.

With an ATM network, data streams of various telecommunication services requiring different bit rates can be transmitted. According to the ATM concept, ATM cells of equal length are formed from various data streams with a digital transmission path which is the same at least across some sections. The structure of the ATM cells is standardised. The cells comprise a cell header of 5 bytes with control information and a payload space of 48 bytes. The control information among other things comprises details concerning the path which the respective cell has to take. Certain ATM service types have been introduced so as to fulfil the requirements of all telecommunication services in ATM networks. The ATM reference model represents the basis for describing these service types.

The ATM reference model is based on the principles of the OSI reference model; it is composed of a user plane, a control plane and a management plane (Gerd Siegmund: "ATM - The technology" 3rd edition Hüthig Publications, Verlag

Heidelberg, pp. 91 - 92. [The aforementioned publication is in the German language, its original title being "ATM - Die Technik".] Figure 1 shows this reference model where the user plane is further divided into the layers "physical layer", "ATM layer", "adaptation layer" and "higher layers for user data", with these layers having to be able to communicate with each other by way of suitable interfaces.

Interface units PHY which permit data transfer tailored to the respective transmission medium, form part of the physical layer.

Utopia Level 2 (The ATM Forum, Technical Committee: Utopia Level 2, Version 1.0 af-phy-0039.000, June 1995) provides a specification of the data path interface between the ATM layer and the interface unit PHY of the physical layer.

An ATM network can contain various devices which, as is the case with the interface units PHY of the physical layer, comprise registers and require a configuration and/or continuous monitoring of register values. For this reason, such devices must provide access for a management device via which configuration and/or monitoring is made possible.

Thus according to the UTOPIA level 2 specification, each of the interface units PHYs comprises a management interface (shown in Appendix 2) which is used by a management unit for configuring, administering and monitoring one or several PHYs. This management interface is in particular configured as a microprocessor interface.

Appendix 2 of Utopia Level 2 proposes a concrete design of management interfaces for interface units PHYs as a guideline for users. Usually this design is used. For example, in the case of a parallel interface, information is provided concerning required and optional interface signals as well as operations and read cycles.

If a management unit is to have access to several devices via its management interface, then connections between the management unit and all these devices must be established by using a bus. For example, an ATM network can comprise hundreds of interface units PHY, leading to considerable costs for these additional management networks.

It is thus the object of the invention to provide an option, for devices associated with an ATM network and comprising registers, for particularly inexpensive reading or writing of data into these registers or from these registers.

According to the invention, this object is met by a process for writing data into registers of at least one device comprising a management interface, involving the following steps:

- composing ATM cells by at least one management unit, with the management unit addressing the ATM cells in each instance to a control unit linked to a data path interface, and integration of instructions associated with particular devices, e.g. writing of data into the registers of the devices, in the form of an operation code, together with the respective information into the payload of the ATM cells;

- transmitting the ATM cells to the addressed control unit via the respective data path interface;

- extracting the operation codes being associated with particular devices, and the associated information in the control unit contained in the payload of the ATM cell; and

- if after the operation code, data is to be entered, setting of the register values of the devices according to the information provided from the ATM cell for this.

This object is also met by a process for reading values from registers of a device comprising a management interface, involving the following steps:

- composing ATM cells by at least one management unit, with the management unit addressing the ATM cells in each instance to a control unit linked to a data path interface, and integrating instructions associated with particular devices, e.g. reading of data from the registers of the devices, in the form of an operation code, together with the respective information into the payload of the ATM cells;

- transmitting the ATM cells to the addressed control unit via the respective data path interface;

- extracting the operation codes being associated with particular devices, and the associated information in the control unit contained in the payload of the ATM cell; and

- if after the operation code, register values are to be read out from devices, reading of the register values

of the respective devices, integration of the read values into ATM cells with addressing to the management unit and transmission of the cells to the management unit.

Likewise, the object is met by a control unit which provides access to the management interface of at least one device comprising registers, as well as to an Utopia bus providing a data path interface of an ATM network, with the control unit being suitable for receiving ATM cells composed by a management unit and destined for the control unit, and extracting and carrying out individual instructions associated with a particular device, in particular reading and/or writing of register data into the devices or from the devices from the payload of these cells, and extracting them and carrying them out in respect of the respective device.

Finally, according to the invention, the object is also met by an ATM cell comprising a cell header of 5 bytes and a payload space of 48 bytes, said cell being used for transmitting management data between a management unit with access to an ATM network and at least one device, with said device comprising registers into which data is to be written and/or from which data is to be read out, and a management interface by way of which a control unit has access to the registers of the device, with the control unit furthermore having access to an Utopia bus providing a data path interface of an ATM network, and being suitable for receiving certain ATM cells composed by a management unit via the data path interface, said data being destined for the control unit, and from the payload of these cells to extract individual instructions associated with a particular device, in particular reading and/or writing of register data into the devices

or from the devices, and to extract associated information and carry it out in respect of the particular device, with the payload space of the ATM cell comprising instruction blocks in which respective bits are provided

- for an operation code which identifies an instruction type such as read, write, no operation;

- for identification of a device to which the instruction in the instruction block is directed;

- which are associated with particular registers integrated in the identified device; and

- for data required for carrying out the instruction;

and a supplementary block (trailer), in which bits are provided

- for identifying the cell type, such as a new cell or a retransmitted cell;

- as a sequential bit which is toggled with each composition of a new cell which does not constitute a repetition;

- for interrupt information; as well as

- for a checksum.

The process according to the invention, the control unit according to the invention and the ATM cell according to the invention provide the advantage in that they allow transmission of management information on the same paths as ATM data over the ATM network. Thus there is no need

for a communications network dedicated to the transfer of management information. This represents a considerable load alleviation for the system design. Thus an ATM inband protocol is used to transmit management information which is required for configuring and/or monitoring units comprising registers, with management interface.

For the processes according to the invention, for which in particular a combined use is provided, for configuring a device, in particular an interface device PHY, as well as for monitoring status conditions and error conditions, which are provided by the device, the management unit reads or writes the register in the device by using the inband protocol.

The ATM cell according to the invention, the processes according to the invention and the control unit according to the invention can be used for configuring, controlling or monitoring not only PHYs but any devices comprising a management interface, in particular a microprocessor interface. For example, memories, micro processors, ATM layer devices or register modules may be considered.

A VPI/VCI address of its own may be allocated to each control unit so that the management unit can address the ATM cells to the control units, as is provided by the processes according to the invention. In cases where the management unit communicates directly with the control unit via an Utopia bus, there is an alternative option of addressing the control unit via a reserved Utopia bus address of the data interface to which the control unit is connected. Analogously, addressing of the management unit takes place via the control unit for a reply via the

ATM address (VPI/VCI) of the management unit or via a reserved UTOPIA address.

In a preferred embodiment of the process the so-called "request-response" protocol is used with the basic operations read out/set. To this effect, each communication is initiated by the management unit by sending instructions to the control unit within the framework of an ATM cell. All cells are confirmed by a reply cell from the control unit to the management unit. In this, the reply cell represents a modified version of the original cell. For addressing with a UTOPIA address, the 5-byte cell header of the received ATM-cell is taken over for the answer cell; otherwise the respective VPI/VCI value of the management unit is set. Furthermore, the original payload of 48 bytes is copied. If the original ATM cell contained a read instruction, then the data read in according to the instructions are inserted into the areas of the response cell provided for this. Before the response cell is sent off, the CRC checksum is calculated anew and appended.

Advantageously, at least part of the contents updated in this way of the ATM cell to be transmitted back to the management unit, is stored in an intermediate memory in case it will be required later. In particular there is a provision for the contents of the entire ATM cell to be stored in the intermediate memory.

To ensure that only the instructions of properly transmitted ATM cells are being carried out, preferably the management unit must not send the next ATM cell to a particular control unit before it has received a response cell from it, or alternatively, before a defined time limit has been exceeded. The defined time limit depends

on the minimum time required for transmitting the cell, processing it in the control unit and transmitting back a response cell. During processing of a cell, the control unit ignores any further incoming cell.

If the specified time has been exceeded, the management unit transmits the ATM cell again. The cell should contain information from which the control unit can detect whether the cell received by the management unit is a cell that has been transmitted for the first time or a cell that has been transmitted repeatedly. Taking into account the last processed cell, the control unit analyses whether the instructions of the cell have already been processed and thus only the last response cell, separately stored in the intermediate memory, needs to be sent to the management unit anew, or whether first of all the instructions contained in the cell need to be carried out. Analyses as to whether or not the instructions of the first cell have already been processed are necessary because reading out register values representing counter readings usually results in the respective counters being reset. Thus these counter readings would no longer be available during renewed readout of the register and are only maintained via an intermediate memory in the control unit.

Preferably the control unit according to the invention is not only able to extract instructions and data from ATM cells received and to ensure that the instructions are carried out, but equally to compose an ATM cell with addressing to a management unit, using register data from devices to which the control unit has access, and to transmit it to the management unit.

Still further-reaching functions of the control unit are imaginable for the future. For example the control unit can autonomously and regularly carry out separately stored instructions based on the same instruction set used by the management unit, and it can independently initiate communication with the management unit by transmitting an ATM cell to said management unit. For example the reserved bits in the supplementary block or a value not otherwise used, of the operation code, can be used to make it possible for such a cell to be identified in the management unit. In this way, effective automatic periodic monitoring data acquisition can be achieved by which the load in the ATM network can also be reduced because there is no need to send recurring information to the devices comprising registers.

The control unit according to the invention should in particular be seen as a component of a management system for an ATM network for configuring and/or monitoring devices. Each of the devices can comprise registers as well as a management interface (in particular, the management interface proposed in Appendix 2 of Utopia Level 2). Apart from the control unit, the management system comprises at least one management unit. The management unit generates the configuration data for the devices and/or processes the values which can be derived from the registers of the devices. In both cases, the management unit provides instructions for those devices which are to be configured or from whose registers values are to be read-out. Subsequently, the instructions and, if need be, the data are composed in the management unit for one or several devices to which the same control unit has access. Such composition occurs as a payload of an ATM cell, with the ATM cell being addressed to the respective control unit.

In a preferred embodiment the control unit has access to more than one device. If the devices are interface devices which provide access to the physical layers of an ATM network, in particular PHYs, then it makes sense if one control device has access to all interface units which are addressable by the data interface with which the control unit is connected. Based on the UTOPIA Level 2 specification, this can be up to 31 interface units.

A preferred division of the payload space of the ATM cell according to the invention consists of providing 4 bytes both for the instruction blocks and for the supplementary block as this provides the necessary and at the same time adequate capacity for the individual spaces. In this way 11 instruction blocks can be transmitted by one ATM cell.

For each of the instruction blocks in the payload space, the ATM cell according to the invention provides space for an operation code with which the command type is determined which is allocated to the respective instruction block. It is advantageous if 2 bits are allocated to the operation code. Thus apart from the instruction types "read" and "write" an instruction type "no operation" can also be used. Such an instruction type is necessary if no complete ATM cell can be filled with instructions. Furthermore, one operation code remains for future applications.

Since in addition it makes sense if an ATM cell sensibly transports instructions for several spatially adjacent devices, one space has been provided for identifying an addressed device. According to the UTOPIA Level 2 specification, up to 31 interface units can be addressed by one data interface so that up to 5 bits are required for identification. However, for the time being an

identification space of 3 bits is adequate because at present, for reasons of space, no more than 8 interface units can be accommodated on one card. In order to fully take into account future extensions, 2 reserve bits can be included. By providing 3 bits for the identification space, an ATM cell according to the invention is generally suitable for communication with 8 freely selectable devices which comprise registers.

In addition, each instruction block of the ATM cell according to the invention comprises an address field for allocation of certain memory locations within the particular device. UTOPIA level 2 specifications prescribe 12 bits for the register addresses so that the entire register contents of a PHY can be addressed with an address field of 12 bits. If according to an advantageous embodiment of the ATM cell a size of 17 bits is provided for the address field, then apart from the entire register contents, a substantial memory area can also be made accessible, e.g. for addressing memory modules.

Eventually, for each of the 11 instruction blocks provided, the ATM cell according to the invention provides an area for management data. According to a preferred allocation of the spaces of the ATM cell, it is provided for each of the data fields to be one byte in size. In this way, conversion of the data into the format required for the UTOPIA parallel management interface can be simplified.

A space for identifying the cell type is reserved for the supplementary block of the ATM cell according to the invention, with 1 bit being sufficient for this. In this space, the management unit can carry out identification

of an ATM cell to be transmitted, with such identification providing information whether this ATM cell is a new cell or a repetition cell. Thus for example when using a bit as a reserved space, in the case of repetition, the bit can be set to "1".

The provided sequential bit is toggled with each new cell. By contrast, in the case of a repetition cell, the sequential bit set is the same as that of the original cell. In this way the sequential bit can be used for evaluation in the case of faulty transmission being detected, as will become clear later on.

In addition a further space of for example 5 bits can be planned in as a reserve.

Many interface units, in particular many PHYs support an interrupt line to be able to signal special events such as an alarm. To meet the purpose of the interrupt lines, the software needs to poll such units to be able to react accordingly if no direct interrupt signalling is possible. The task of the software is simplified if the entire situation of the interrupt requirements of the units connected to the control unit is monitored. For this reason, the supplementary block of the ATM cell according to the invention comprises an interrupt field. This field can be updated with each new ATM cell which is transmitted. With an identification space of the addressed units of 3 bits, the interrupt field preferably comprises 8 bits so that an interrupt field in the supplementary block can be allocated to each of the 8 addressable units according to the allocation of the values in the identification area. In addition, the 5 reserve bits of the supplementary block can be used for future expansion of the interrupt field.

As there is always the possibility of errors occurring during transmission of a message, some check of corruptions should exists. For this reason an area of the supplementary block has been set aside for a checksum. After receipt of a new ATM cell, both the management unit and the control unit can thus carry out a checksum verification and discard the cell if the check indicates an incorrect transmission. The checksum is in particular formed across the entire payload.

In a preferred embodiment of the ATM cell according to the invention, prior to transmission of each cell a CRC-10 remainder is appended to each cell as the last 10 bits. In order to simplify the hardware design, the checksum is formed across all bytes of the payload except for the last 2 bytes of the supplementary block, i.e. across a total of 46 bytes. Thus 6 bits of the supplementary block (2 bytes minus 10 bit checksum) are not protected from corruption. In respect of the algorithm used it is assumed that these 6 bits are constantly set to "0", but the algorithm can be freely available.

Preferably a big-endian sequence is used for the payload area of the ATM cell according to the invention, so that the last byte of the 48 byte payload is the low-order byte of the twelfth 32-bit word of the payload. But it is also possible to select the "little endian" sequence.

The use of the first process according to the invention or control unit according to the invention or the ATM cell according to the invention, is particularly advantageous for configuring interface units which represent access to the physical layers. But it is

exactly such interface units where the invention can also be used for regular acquisition of performance data and statistical data of the interface unit, by way of the control unit, by using the second process according to the invention. To do so, it is always the same instruction set which is used.

Further advantageous embodiments of the invention are described in the dependent claims.

Below, the invention is described in more detail by means of embodiments referring to drawings. The following are shown:

Fig. 1: the ATM reference model;

Fig. 2: the integration of a control unit according to the invention, in an ATM network;

Fig. 3: the ATM cell format used;

Fig. 4a: the bit division, according to the invention, of the instruction blocks; and

Fig. 4b: the bit division, according to the invention, of the supplementary block.

A reference to Figure 1 has already been provided in the introduction.

Figure 2 shows part of a typical ATM network environment. A management unit 1 as well as interface units (PHY) 4 integrated in a line card 3, of the physical layer, form part of an ATM network, respectively. The "cloud" 2 shown

represents the layers ATM, AAL and "higher layers" of the network.

The management unit 1 comprises a timer.

By way of a Utopia data path interface 7, the interface units 4 have access to an ATM layer device (not shown) of the ATM network 2. Furthermore, the interface units 4 comprise a management interface 6. The path of the user data, from the interface units to the transmission medium, is indicated by dotted lines 8.

In addition to these elements, a control unit 5 (CLIC: control link circuit) has been provided which together with the interface units 4 is integrated in the line card 3. The control unit 5 is also connected to the Utopia data path interface 7 as well as with the management interface 6 of the interface units 4. There is also an intermediate memory (not shown) of the control unit 5.

The management unit 1 provides management data for the interface units 4. The management data comprises instructions to be carried out, with each instruction being associated with a particular interface unit 4. From the management unit 1 to the respective control unit 4, this management information is to take the same path through the network as does the ATM-user data flow. The management information thus needs to be packed into ATM cells with addressing to the respective control unit contained in the cell header. With each ATM entity to traverse, the next path section is determined from the cell header information and the cell is forwarded along said path section via the transmission medium, until it reaches the ATM entity with the addressed control unit 5.

From the point of view of the ATM, the control unit 5 behaves like an interface unit 4 which is accessible via a data path interface 7.

The control unit 5 is able to detect ATM cells addressed to it. If such a line comes in, the control unit 5 takes the data from the cell, evaluates the information received and carries out the intended instructions via the management interfaces 6.

The management unit can have access to the OAM cell stream and can thus generate CLIC cells from OAM cells, or it can generate OAM cells from the data collected via inband protocol by the PHYs, and it can send these cells to other management units via the ATM-network.

The actions requested via the instructions can in part consist of the setting of certain registers of a particular interface unit 4, or of the values of the registers of the interface unit 4 being read-out.

Figure 3 shows the general structure of an ATM cell used for management information; hereafter it will be referred to as a CLIC cell.

Like every ATM cell, the CLIC cell too comprises a cell header of 5 bytes and a payload space of 48 bytes with the cell header among other things comprising information concerning the path (VPI/VCI).

In a CLIC cell, the payload space is divided into 11 instruction blocks of 4 bytes each as well as a supplementary block (trailer) of 4 bytes. With every instruction block, a single instruction can be transmitted.

Figure 4a shows the structure of the 4-byte instruction blocks; said structure always remains the same. The bits of the instruction block shown are consecutively numbered from 0 to 31.

Bits 30 and 31 (OP) are reserved for the entry of an operation code. By way of possible operation codes, the following have been provided: '00' for "no operation" (NOP), '01' for "read", '10' for "write". Code '11' is kept free.

Bits 28 and 29 (R) have been kept free in reserve.

Three bits (25 - 27) have been provided as "device select" bits DS for identification of the interface unit 4 to which the instruction block relates. Thus up to eight interface units 4 can be configured by the control unit 5.

Furthermore, the bits 8 - 24 are for the register addresses of the addressed interface unit 4. With these 17 bits, all registers of an interface unit 4 can be allocated individually.

Finally, one byte (bits 0 - 7) has been provided for the data which provides the basis for carrying out instructions.

Figure 4b shows the structure of the supplementary block of the CLIC cell which in the payload space adjoins the 11 instruction blocks. The supplementary block also comprises 4 bytes.

Bit 31 is used for setting a cell type identification (flag). If this bit is not set, the CLIC cell is a new cell. By contrast, if it is set, the cell is a cell sent again.

A sequential bit (bit 30) adjoins the bit for the cell type. This bit is toggled from one cell to the next, except in the case of a repetition cell. In the case of a repetition cell, the value of the last sequential bit is repeated, too.

Bits 24 - 29 are kept in reserve. 8 bits (16 - 23) for interrupts (int0 - int7) follow the maximum of eight interface units 4. It makes sense if allocation of the interrupts int0 - int7 corresponds with allocation of the interface units for the values 1 - 8, which can be set via the 3 bit DS field. If the condition of further interrupts is to be monitored, then the six reserve bits can be used for this purpose.

The bits 10 - 15 of the supplementary block are constantly set to '0'.

A 10 bit checksum (CRC 10) can be inserted into the last bits 0 - 9 of the supplementary block and thus also the CLIC cell.

According to the invention, the division of the CLIC cells provided according to Figures 3 and 4 not only makes it possible to exchange instructions by means of "in-band" transmission between a management unit 1 and interface units 4, but it also makes it possible to provide a reliable process if errors occur.

The process used is a request-response process. After the instructions received have been carried out, each cell sent from the management unit 1 to the control unit 5 is sent back to the management unit 1 in a modified form. In this way, the management unit 1 receives confirmation that the instructions were able to be processed by the control unit 5. In addition, the results of "read" instructions can be introduced to these response cells, said instructions having resulted from the reading of data, by the control unit 5, from the registers of the addressed interface units 4.

Both in respect of the request cell of the management unit 1 and in respect of the response cell of the control unit 5, a checksum is determined and deposited in the last 10 bits of the supplementary block, before the CLIC cell is transmitted. The polynomial $x^{10} + x^9 + x^5 + x^4 + x + 1$ is used to determine the checksum (CRC 10 remainder). This polynomial is for example also provided for in the ATM-OAM specifications (ITU-T I.610, "Common OAM cell fields" p. 27). The checksum is formed across all bytes of the payload except for the last 2 bytes of the supplementary block, i.e. the area assumed to be set to '0' and the checksum area itself. When the CLIC cell is received in the management unit 1 or in the control unit 5, this checksum is first compared with a sum formed anew in the reception unit via the payload. Further processing will only take place if there is agreement; otherwise the cell is discarded.

The timer of the management unit 1 and the memory of the control unit 5 are provided as a safeguard in case processing of the instructions is not successful or in case of faulty transmission of a CLIC cell. The timer of the management unit 1 is always started when a CLIC cell

is put out. By means of the timer it is thus possible to monitor whether a specified time limit, between transmission of the CLIC cell to receiving a response cell, has been exceeded.

This time limit can be reached if monitoring of the checksum has shown an error either by the management unit 1 or by the control unit 5, and if the CLIC cell concerned was discarded. In this case the management unit 1 resends the last CLIC cell, while maintaining the last-used value of the sequential bit. This indicates that the cell is a repetition cell, because the bit of the cell type recognition (bit 31) of the supplementary block is set to '1'. If the control unit 5 detects that the cell type bit has been set, then it compares the status of the sequential bit of the CLIC cell received with that of the preceding CLIC cell, which has been stored in the intermediate memory of the control unit 5.

If the sequential bits are different, this indicates an error detection on the receiving side and cell discarding during checksum verification in the control unit 5. Thus the CLIC cell has not yet been processed by the control unit 5. The commands of the repetition cell are carried out as if it were a new CLIC cell. Also, a response cell is regularly formed and transmitted to the management unit 1.

By contrast, if the sequential bits are identical, this indicates an error detection on the receiving end and cell discarding during checksum verification in the management unit 1. It is thus assumed that correct implementation of the instructions of the cell has already taken place, with the response cell having been lost on the way back to the management unit 1. In this

case only the content of the intermediate memory in the control unit 5 is read out and sent back to the management unit 1.

Reading from the intermediate memory is necessary because the cell transmitted to the management unit 1 also contains data read out from the interface units 4, for example performance data, corresponding to a current counter state in the interface unit 4. As soon as such a counter value has been read out, usually the interface unit 4 resets the counter. In the case of renewed read-out of the register values which represent the counter status, the new counter status would be transmitted for a regular new creation of a response cell, and thus from the point of view of allocation, an incorrect value would be transmitted to the management unit 1.

Exceeding the time limit can also occur if a cell has been delayed in a data jam. In such a case the response cell may arrive late in the management unit 1, after the repetition cell has already been dispatched, so that subsequently a further response cell 5 is received by the control unit. The management unit 1 is thus able to differentiate which cells have been received. One of the two cells can then be discarded since both cells have the same content.

CLAIMS

1. A process for writing data into registers of at least one device (4) comprising a management interface (6), characterised by the following steps:

- composing ATM cells by at least one management unit (1), with the management unit (1) addressing the ATM cells in each instance to a control unit (5) linked to a data path interface (7), and integration of instructions associated with particular devices (4), e.g. writing of data into the registers of the devices (4), in the form of an operation code, together with the respective information into the payload of the ATM cells;

- transmitting the ATM cells to the addressed control unit (5) via the respective data path interface (7);

- extracting the operation codes being associated with particular devices (4), and the associated information in the control unit (5) contained in the payload of the ATM cell; and

- if after the operation code, data is to be entered, setting of the register values of the devices (4) according to the information provided from the ATM cell for this.

2. A process for reading values from registers of a device (4) comprising a management interface (6), characterised by the following steps:

- composing ATM cells by at least one management unit (1), with the management unit (1) addressing the ATM cells in each instance to a control unit (5) linked to a data path interface (7), and integrating instructions associated with particular devices (4), e.g. reading of data from the registers of the devices (4), in the form of an operation code, together with the respective information into the payload of the ATM cells;

- transmitting the ATM cells to the addressed control unit (5) via the respective data path interface (7);

- extracting the operation codes being associated with particular devices (4), and the associated information in the control unit (5) contained in the payload of the ATM cell; and

- if after the operation code, register values are to be read out from devices (4), reading of the register values of the respective devices (4), integration of the read values into ATM cells with addressing to the management unit (1) and transmission of the cells to the management unit (1).

3. A process according to claim 1 or 2, c h a r a c t e r i s e d i n t h a t the devices (4) are ATM interface units of the physical layer by means of which a data path

interface (7), in particular UTOPIA, provides access for the ATM layer to a physical transmission medium.

4. A process according to one of the preceding claims, characterised in that addressing of ATM cells to the control unit (5) by the management unit (1) takes place via a VPI/VCI address associated with the control unit (5), or if the management unit (1) communicates directly with the control unit (5), via an UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

5. A process according to one of the preceding claims, characterised in that addressing of ATM cells to the management unit (1) by the control unit (5) takes place via a VPI/VCI address associated with the management unit (1), or if the management unit (1) communicates directly with the control unit (5), via a UTOPIA data interface (7), addressing takes place via a reserved UTOPIA bus address of the data interface (7).

6. A process according to one of the preceding claims, characterised in that transmission of the ATM cells is based on the request-response protocol.

7. A process according to claim 6, characterised in that the management unit (1) does not send any further ATM cells to a control unit (5) as long as it has not received a correct response to the preceding ATM cell from said control unit (5), or as long as a time limit has not been exceeded.

8. A process according to one of the preceding claims, characterised in that prior to any forwarding of ATM cells destined for the management unit (1), the control unit (5) forms a checksum, and prior to any forwarding of ATM cells destined for a control unit (5), the management unit (1) forms a checksum, across at least part of the payload of the ATM cell, in particular a CRC-10 sum, and integrates this sum into the ATM cell to be transmitted.

9. A process according to one of the preceding claims, characterised in that prior to carrying out any instructions, the control unit (5) checks a checksum transmitted with the ATM cell received, and carries out the instructions only if no transmission error is detected; otherwise it discards the ATM cell and is ready to receive new ATM cells.

10. A process according to claim 9, characterised in that after each processing of the instructions of an ATM cell, the control unit (5) places at least part of the updated content of the cell to be transmitted to a management unit, in particular the updated content of the entire cell, into an intermediate memory.

11. A process according to one of claims 8 - 10, characterised in that
- after a specified time limit after sending a first ATM cell addressed to a control unit (5) has lapsed and prior to receiving a response ATM cell from the control unit (5) with a correct CRC sum,

the management unit (1) sends the same ATM cell again, identifying it as a repetition cell;

- when receiving a repetition cell, the control unit (5) checks whether or not, following the first ATM cell, a response ATM cell was transmitted to the management unit (1); and

- if no, processes the instructions contained in the cell; or

- if yes, retransmits the response ATM cell which has already been sent once and which has been stored separately, to the management unit (1).

12. A process according to one of the preceding claims, characterised in that for each ATM cell to be composed, the control unit (5) maps the current interrupt state of the connected devices (4) into interrupt bits provided for this purpose in the payload of the ATM cell.

13. A process according to one of the preceding claims, characterised in that the control unit (5) autonomously and regularly reads in data from devices (4) connected to it and transmits such data, integrated into ATM cells, to the management unit (1).

14. A control unit (5) providing access to the management interface (1) of at least one device (4) comprising registers as well as to a data path interface (7) of an ATM network, with the control unit (5) being suitable for receiving ATM cells composed by a management unit (1) and destined for

the control unit (5) via the data path interface (7), and extracting and carrying out individual instructions associated with a particular device (4), in particular reading and/or writing of register data into the devices (4) or from the devices (4) from the payload of these cells and extracting them and carrying them out in respect of the respective device (4).

15. A control unit (5) according to claim 14, characterised in that the management interface (6) corresponds to the management interface proposed in Appendix 2 of Utopia Level 2.

16. A control unit (5) according to claim 14 or 15, characterised in that the data path interface (7) corresponds to the data path interface specified in Appendix 2 of Utopia Level 2.

17. A control unit (5) according to one of claims 14 - 16 characterised in that it is suitable for composing the register data read from the registers of the devices (4) to become ATM cells, address it to a management unit (1) by means of the VPI/VCI address of the management unit (1), or address it using a UTOPIA address reserved for inband communication, and forward it to the data path interface (7).

18. A control unit (5) according to claim 17, characterised in that it comprises an intermediate memory for storing at least part of the content of the ATM cell to be transmitted to the management unit (1).

19. A management system for an ATM network for configuring and/or monitoring devices (4) comprising registers and a management interface (6), respectively, with the management system comprising control units (5) according to one of claims 14 - 18, as well as at least one management unit (1) suitable for generating configuration data for the devices (4) and/or for processing the data available from the registers of the devices (4), with the management unit (1) being suitable for generating instructions for a particular device (4) respectively, for joining instructions and data for one or several devices (4) to which the same control unit (5) has access, as a payload of an ATM cell and for addressing the ATM cell to the respective control unit (5).

20. A management system according to claim 19, characterised in that the devices (4) comprising registers are connected to a unit of the ATM layer of the ATM network via the data path interface (7).

21. A management system according to claim 19 or 20, characterised in that the devices (4) comprising registers are ATM interface units of the physical layer, in particular PHYs, by way of which the ATM layer of the ATM

network has access to at least one transmission medium.

22. A management system according to claim 21, characterised in that the control unit (5) has access to management interfaces (6) of up to 31 interface units (4).

23. An ATM cell comprising cell header of 5 bytes and a payload space of 48 bytes, said cell being used for transmitting management data between a management unit (1) with access to an ATM network and at least one device (4), with said device (4) comprising registers into which data is to be written and/or from which data is to be read out, and a management interface (6) by way of which a control unit (5) has access to the registers of the device (4), with the control unit (5) furthermore having access to a data path interface (7) of an ATM network, and being suitable for receiving certain ATM cells composed by a management unit (1) via the data path interface (7), said data being destined for the control unit (5), and from the payload of these cells to extract individual instructions associated with a particular device (4), in particular reading and/or writing of register data into the devices (4) or from the devices (4), and to extract associated information and carry it out in respect of the particular device (4), with the payload space of the ATM cell comprising instruction blocks in which respective bits are provided

- for an operation code which identifies an instruction type such as read, write, no operation;

- for identification of a device (4) to which the instruction in the instruction block is directed;

- which are associated with particular registers integrated in the identified device (4); and

- for data required for carrying out the instruction,

and a supplementary block (trailer), in which bits are provided

- for identifying the cell type, such as new cell or a retransmitted cell;

- as a sequential bit which is toggled with each composition of a new cell which does not constitute a repetition;

- for interrupt information; as well as

- for a checksum.

24. An ATM cell according to claim 23, c h a r a c t e r i s e d i n t h a t 11 instruction blocks and a supplementary block of 4 bytes each are used in each payload space.

25. An ATM cell according to claim 24, c h a r a c t e r i s e d i n t h a t for each of the 11 instruction blocks the following are provided

- for the operation code 2 bits;

- for identification of the device (4) 3 - 5 bits and, supplementing to 5 bits for reserve, 0 - 2 bits;

- for allocation of the registers 17 bits;

- for the data required to carry out a respective instruction 1 byte;

and that for the supplementary block the following are provided

- for identification of the cell type 1 bit;

- as a sequential bit 1 bit;

- additionally as a reserve 5 bits;

- for the interrupt information 1 byte; and

- for the checksum, formed by a cyclic redundancy check (CRC), 10 bits.

26. An ATM cell according to one of claims 23 - 25, characterised in that a "big endian order" is used.

27. The use of an ATM cell according to one of claims 23 - 26 for configuring ATM interface units (4) of the physical layer.

28. The use of an ATM cell according to one of claims 23 - 26 for the reading out of data, available in the

ATM interface units (4) of the physical layer, in particular register values.

ABSTRACT

The invention relates to a process for writing data into registers of at least one device (4) comprising a management interface (6), or a process for reading values from registers of such devices (4). To provide an option for particularly inexpensive reading or writing of data, communication between at least one management unit (1) which generates the data to be written or which undertakes further processing of read-out data, and the control units (5) by means of the ATM inband protocol, is proposed. The control units (5) which have access to the registers of at least one of the devices (4) by way of the management interface (6), receive ATM cells addressed to them from the management unit (1), with instructions and information for specific devices (4) connected to the respective control unit (5) being integrated into the payload of said ATM cells. The control units (5) carry out the instructions and if applicable transmit a response ATM cell back to the management unit (1). The invention also relates to a control unit as well as an ATM cell for carrying out read and write operations by means of the inband protocol.

Figure 2 has been provided for publication.

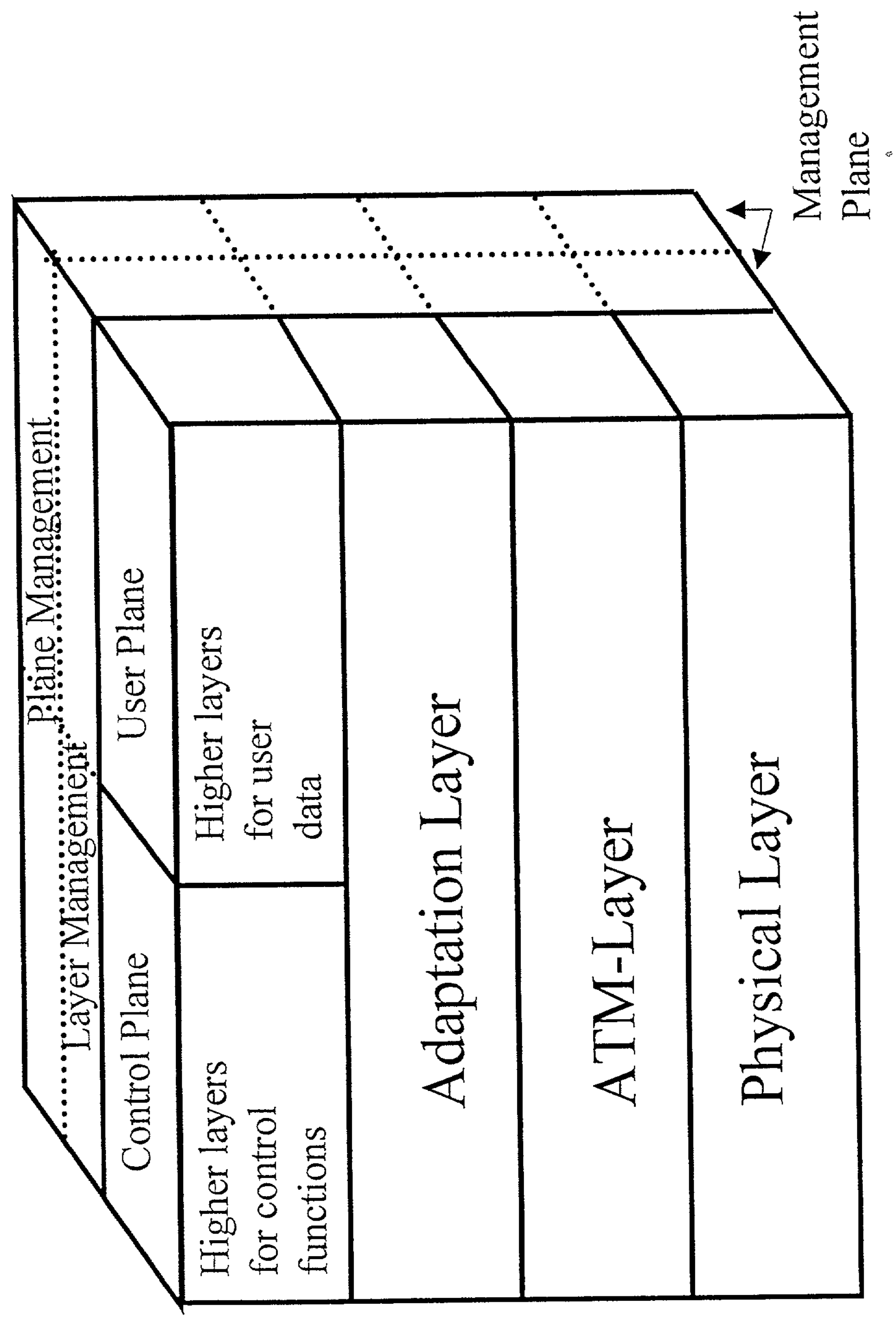
Management Plane
Plane Management
Layer Management
Control Plane
User Plane
Higher layers for control functions
Higher layers for user data
Adaptation Layer
ATM-Layer
Physical Layer

Fig. 1

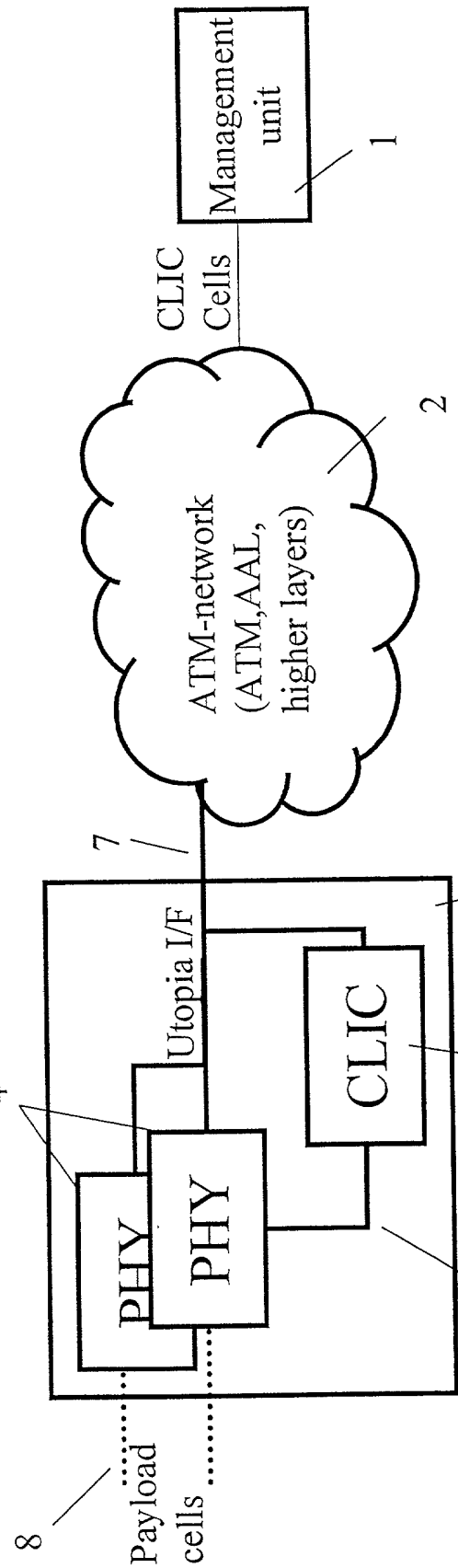
Management unit
1
CLIC Cells
ATM-network (ATM,AAL, higher layers)
2
7
Utopia I/F
3
4
PHY
PHY
CLIC
5
6
8
Payload cells

Fig. 2

| - Byte -| -Byte-| -Byte-| -Byte- | - Byte-

ATM cell header	HEC
Instruction word 1	
Instruction word 2	
Instruction word 3	
Instruction word 4	
Instruction word 5	
Instruction word 6	
Instruction word 7	
Instruction word 8	
Instruction word 9	
Instruction word 10	
Instruction word 11	
Supplementary word	

FIG. 3

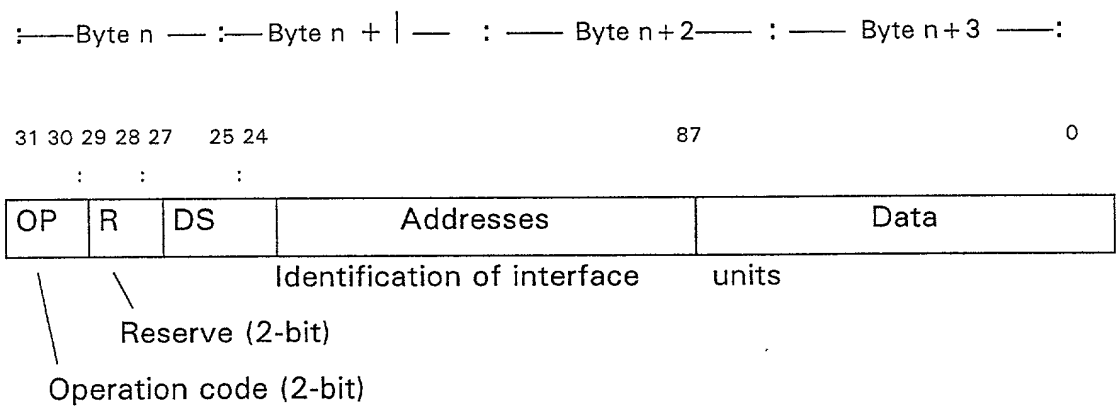
Byte n
Byte n + 1
Byte n+2
Byte n+3
31 30 29 28 27
25 24
87
0
OP
R
DS
Addresses
Data
Identification of interface units
Reserve (2-bit)
Operation code (2-bit)

FIG. 4a

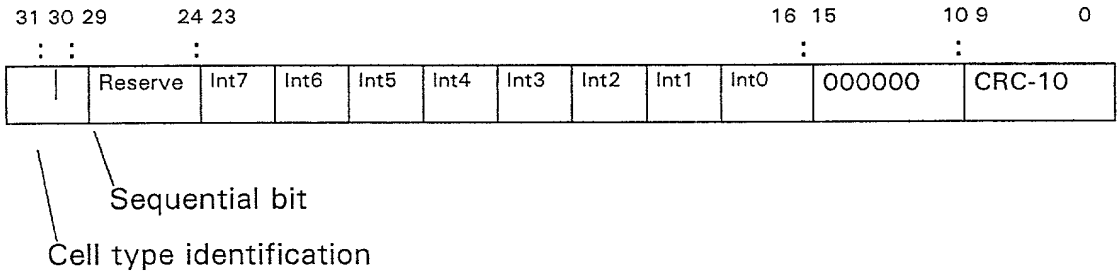
31 30 29
24 23
16 15
10 9
0
Reserve
Int7
Int6
Int5
Int4
Int3
Int2
Int1
Int0
000000
CRC-10
Sequential bit
Cell type identification

FIG. 4b

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY Includes Reference to PCT International Applications	Attorney's Docket No.4925-131PUS

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

AN ATM INBAND PROTOCOL

the specification of which (check only one item below)

[] is attached hereto

[] was filed as United States application

Serial No. _

on _

and was amended

on _ (if applicable).

[] was filed as PCT international application

Number PCT/EP00/00116

on 11 January 2000

and was amended under PCT Article 19

on _ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

PRIOR FOREIGN/PCT APPLICATIONS AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

Country (if PCT, indicate "PCT")	Application Number	Date of Filing (day, month, year)	Priority Claimed Under 35 U.S.C. 119	
Germany	199 02 436.7	22 January 1999	[x] YES	[] NO
PCT	PCT/EP00/00116	11 January 2000	[x] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO

(Includes Reference to PCT International Applications)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS *(check one)*		
U.S. APPLICATION NUMBER	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO.	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED *(if any)*			
PCT/EP00/00116	11 January 2000			X	

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*List name and registration number*)

14 MYRON COHEN, Reg. No. 17,358; THOMAS C. PONTANI, Reg. No. 29,763; LANCE J. LIEBERMAN, Reg. No. 28,437; MARTIN B. PAVANE, Reg. No. 28,337; MICHAEL C. STUART, Reg. No. 35,698; KLAUS P. STOFFEL, Reg. No. 31,668; EDWARD M. WEISZ, Reg. No. 37,257; JULIA S. KIM, Reg. No. 36,567; VINCENT M. FAZZARI, Reg. No. 26,879; ALFRED W. FROEBRICH, Reg. No. 38,887; KENT H. CHENG, Reg. No. 33,849; ROGER S. THOMPSON, Reg. No. 29,594; GEORGE J. BRANDT, JR., Reg. No. 22,021; F. BRICE FALLER, ~~Reg. No.~~ No. 29,532 and YUNLING REN, Reg. No. 47,019,

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201	FULL NAME OF INVENTOR	FAMILY NAME STORCK	FIRST GIVEN NAME Hubertus	SECOND GIVEN NAME
	RESIDENCE, CITIZENSHIP	CITY Düsseldorf	STATE OR FOREIGN COUNTRY Germany DE	COUNTRY OF CITIZENSHIP Germany
	POST OFFICE ADDRESS	POST OFFICE ADDRESS ~~Füllenbachstr. 5~~ Am Forst Kalkum 11	CITY Düsseldorf	STATE & ZIP CODE/COUNTRY ~~D-40474~~ D-40472
202	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE, CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

203	FULL NAME OF INVENTOR	FAMILY NAME	FIRST GIVEN NAME	SECOND GIVEN NAME
	RESIDENCE, CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS	CITY	STATE & ZIP CODE/COUNTRY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
Lubotus Stark		
DATE 8/16/2001	DATE	DATE

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY Includes Reference to PCT International Applications	Attorney's Docket No.**4925-131PUS**

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			[] YES	[] NO
			[] YES	[] NO
			[] YES	[] NO

Combined Declaration for Patent Application and Power of Attorney (Continued) (Includes Reference to PCT International Applications)	Attorney's Docket No. **4925-131PUS**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

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U.S. APPLICATIONS		STATUS *(check one)*		
U.S. APPLICATION NUMBER	U.S FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.					
PCT APPLICATION NO	PCT FILING DATE	U.S. SERIAL NUMBERS ASSIGNED *(if any)*			
PCT/EP00/00116	11 January 2000			x	

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Combined Declaration for Patent Application and Power of Attorney (Continued) (Includes Reference to PCT International Applications)				Attorney's Docket No. 4925-131PUS
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DATE	DATE	DATE